REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-16 are pending in the application. Claims 1 through 10 and 12 through 16 have been rejected. Claim 11 have been objected to. Claims 1, 8, 12 through 16 have been voluntarily amended for clarification purposes only

The above mentioned claims amendments were not made in response to any cited prior art, nor do they introduce any new matter to the application.

CLAIM REJECTIONS

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claim 12 under 35 U.S.C. § 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has currently amended claim 12 to overcome this rejection.

35 U.S.C. § 102 Rejections

In the office action the Examiner had rejected independent claims 1, 8 and 13 under 35 USC 102(a) as being anticipated by Lakhani et al US 2003/0126385(the '385 reference). Applicant respectfully traverses this rejection because the examiner has failed to establish a case of anticipation. More specifically, the cited reference does not teach all the limitations of independent claims 1, 8 and 13. The cited reference does not teach all of the limitations of

independent claims 1, 8 and 13 (as filed). In the interest of expediting the prosecution of the present application, however, Applicant has voluntarily amended claims 8 and 13 to better highlight the distinctions of these claims from the cited prior art, which prior art actually teaches away from the claimed subject matter.

In the Office Action, the Examiner stated that Lakhani et al (the '385 reference), discloses *"a method for operating a non-volatile memory device comprising: using one or more unused bits of an address argument (Lakhani's page 7 table A, C1, C2 bits) of a command as an addressing mode field... "*.

After careful examination of the cited reference, it would appear that there has been a misinterpretation of certain portions of the cited reference, namely the nature of bits C1 and C2 disclosed in the '385 reference, which in fact are control signals. C1 and C2 are control signals and are an integral part of the control-flow of the controller disclosed in the '385 reference.

Contrary to the teachings of '385 reference, claim no.1 (as originally filed and after amendment) of the pending application recites: ***"using one or more unused bits of an address argument of a command as an addressing mode field".*** Independent claims 8 and 13, as filed included the same limitation by implication, but have since been amended to expressly recite this limitation. Thus, the pending application claims a novel apparatus, method and code to operate a non-volatile memory device in byte address mode or in block address mode, **using an unused portion of the address argument** and without the use of additional control signals within the existing controller, as taught by the '385 reference.

The pending independent claims recite:

- Claim no. 1 of the pending application cites:

  "A method for operating a non-volatile memory device comprising: ***using one or more unused bits of an address argument of a command as an addressing mode field*** *to determine whether said address argument is a byte address argument or a block address argument."*

- Claim no.8 of the pending application cites:

"An apparatus comprising: a non-volatile memory unit; and a controller adapted to ***use one or more unused bits of an address argument of a command as an addressing mode field*** *to determine whether an addressing mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode."*

- Claim no.13 of the pending application cites:

"a storage medium having stored thereon instructions that, when executed by a computing platform functionally associated with a non-volatile memory device, result in: ***using one or more unused bits of an address argument of a command as an addressing mode field*** *to determine whether said address argument is a byte address argument or a block address argument."*

Whereas, the cited reference teaches (away):

- Page 10, of the '385 reference recites in part:

*"****The individual cells of array 16 of Fig.1 are addressed by address bits A(22:0) and AX,*** *with the four highest order address bits (A22, A21, A20 and A19) determining the main block, the three next highest order bits (A18, A17 and A16) determining the erase block, the address bit (A15) determining the sector, the next four address bits (A(8:5)) and bit AX determining the packet (within the sector), and the five lowest order address bits (A(4:0)) determining the byte within the packet."*

- Page 16, of the '385 reference recites in part:

*"...A preferred embodiment of the system of the invention will be described with reference to Figs. 2-8... system 30 includes controller or control engine 129 (rather then controller 29 of Fig.1)....****Controller 129 can be designed and programmed identically to controller 29*** *of Fig. 1, except that in accordance with*

the invention it has the additional capability to load register 40 and 41 and to control predecoder 50... to assert multiblock selection bits..."

- Pages 18 and 19 of the '385 reference recites in part:

"...The individual cells of the preferred implementation of array 16 (of Fig.2) are ***addressed by address bits A(22:0) and AX in the same manner*** *of as are the cells of the above-described preferred implementation of array 16 of Fig.1...An important advantage of the Fig.2 system over the Fig.1 system is that* ***predecoder 50 is also operable in second mode...Predecoder 50A operates in response to control signal C1 and C2 from controller 129...predecoder 50B operates in response to control signals C3, C4 and C5 from controller 129...***"

- Pages 20 and 21 of the '385 reference recite in part:

"...When precoder 50A operates in a first mode (in response to each of control signal C1 and C2 having the value "0").... When precoder 50A operates in a second mode (in response to control signal C1 having the value "1", regardless of the value of C2)...."

It should be clear to one of ordinary skills in the art that the invention disclosed in the '385 reference teaches a method of accessing memory cells in several modes, all of which modes use control signals, as explicitly pointed out hereinabove and also in the '385 reference abstract, which recites in-part : "...Control lines activate a number of modes...". Moreover, the '385 reference discusses the selection of cells using ***address bits A(22:0) and AX***, which address bits are the address argument and are not the control signals which are used for the selection of operation mode.

Applicant requests the Examiner to withdraw his 102 rejection of independent claims 1, 8 and 13. Applicant considers claims 1, 8 and 13 allowable over the cited reference. Applicant considers all the claims depending there-from to be allowable by virtue of their dependence on allowable base claims 1, 8 and 13. In view of the foregoing amendments and remarks, all pending claims are considered by Applicant to be allowable. Their favorable reconsideration and allowance is respectfully requested.

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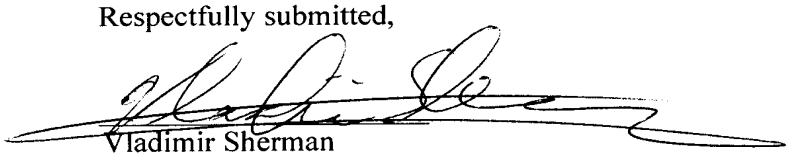
Respectfully submitted,



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